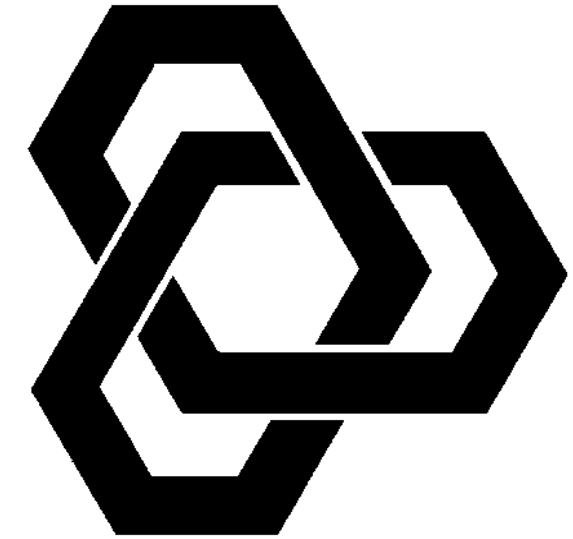
TAMS PCI GPIO Card



Installation & Operation Instructions

TAMS 61622 PCI GPIO Card
Instructions and Software License

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Contents

Unpacking Your Product

When you open your TAMS GPIO Card shipment, examine its contents. Do not remove the GPIO card from its protective bag yet. Make sure your shipment contains the following items:

622-66501	GPIO Card
61622-90003	Installation & Operation Instructions
61622-0101	Software CD
4001	Product Registration Card

Please complete the registration card and return it to TAMS.

Overview and General Information

This guide explains how to install, configure, and utilize enhancements of the TAMS 61622 GPIO (General Purpose Input Output) interface.

GPIO is a parallel interface that is flexible and allows a variety of custom connections. A PCI expansion slot is required to accommodate the GPIO interface card.

The TAMS 61622 card has a rotary switch on the upper edge that is not used in systems running Windows NT4 / 2000 / XP. The configuration of the card, in Windows, is completely done in software.

Since the configuration of the GPIO interface is done in software, rather than using DIP-switches or jumpers, this guide also provides an explanation of the configuration process as it relates to the HP/Agilent Standard Instrument Control Library (SICL). A detailed description of the TAMS 61622's functionality is included to aid in this configuration process.

The TAMS 61622 provides 16 bit data exchange with peripheral devices that do not support more common interface protocols like HP-IB or RS-232. Connection flexibility is augmented in the TAMS 61622 GPIO interface by extra status and control lines, a choice of handshake methods, several data-latching options, and selectable data width and polarity.

There are two basic modes for the data ports in the TAMS 61622 GPIO interface. The TAMS 61622 can be configured like an HP 98622 GPIO interface, which is called *Compatibility Mode*. Alternately, the TAMS 61622 can be configured with a bi-directional data port and auxiliary control lines, which is called *Enhanced Mode* and supported by HP 2074/5.

Installing the GPIO Interface

This section explains how to install the TAMS 61622 GPIO interface in the computer. To complete the installation:

1. Make sure the computer power switch is off.
2. Refer to the Owner's Guide of your computer for instructions on opening your computer and installing PCI boards.
3. Install the GPIO interface in the PC by plugging the card into the PCI slot. Make sure that the card is firmly seated in the slot.

   Follow the instructions being careful to handle the TAMS 61622 board only by its metal bracket. Avoid contact with the edges. After the board has been plugged in and the retaining screw installed the computer should be reassembled.
4. Prepare and install the GPIO interface cable.

Note: The TAMS 61622 is a PCI device. Unlike most EISA and ISA devices a PCI device does not require an I/O address or IRQ setting. These settings are handled automatically.

Related Software Documentation

HP/Agilent Standard Instrument Control Library for Windows (SICL)

To configure the TAMS 61622 GPIO interface for the HP/Agilent Standard Instrument Control Library (HP/Agilent SICL) for Windows, see the “Installing and Configuring the HP/Agilent I/O Libraries” chapter of the *HP/Agilent I/O Libraries Installation and Configuration Guide for Windows*.

To develop HP/Agilent SICL I/O applications for the TAMS 61622 on a PC, see the “Using GPIO with HP/Agilent SICL” chapter of the *HP/Agilent SICL User’s Guide for Windows*. HP/Agilent SICL functions, including those that are GPIO specific, are fully described in the HP/Agilent SICL Reference Manual.

Driver Installation

Driver installation assumes basic knowledge about software installation procedures specific to the platform. Refer to your platform specific operating system documentation or contact your system administrator.

To install the t61622 driver it is not necessary for the TAMS 61622 interface card(s) to be present in the system. Configuration, however, requires the card(s) and driver to both be present.

Important! The HP/Agilent IO libraries (SICL) or HTBasic for Windows needs to be installed before you proceed with the TAMS 61622 GPIO card driver installation.

Windows NT 4.0 Installation

1. Make sure you have privileges enabling you to install device drivers.
2. Insert the CD with the t61622 driver into the CD-ROM drive.
3. Run “setup.exe” from the CD directory “NT4_VERx.xx”.
4. Follow the instructions on the screen displayed by the setup utility.
5. Follow the instructions on page 15, in the section titled: **Configuring the Card in Windows NT4.0 / 2000 / XP**

Windows 2000 installation

After installing the card and booting for the first time the Windows 2000 plug and play manager will detect the new hardware (TAMS GPIO card), the screen looks like this:

Click on cancel.

1. Make sure you have privileges enabling you to install device drivers.
2. Insert the CD with the t61622 driver into the CD-ROM drive.
3. Run “setup.exe” from the CD directory “W2K_VERx.xx”.
4. Follow the instructions on the screen.

You may or may not get the following message:

5. Click on Yes and/or Next and continue with the instructions on the screen.
6. Finally, the installation program will ask you to reboot your PC. Please go ahead and do so.
7. After reboot your TAMS 61622 GPIO card should be ready to be configured.

Now, please follow the instructions on page 15, in the section titled: **Configuring the Card in Windows NT4.0 / 2000 / XP**

Windows XP installation

After installing the card and booting for the first time the Windows XP plug and play manager will detect the new hardware (TAMS GPIO card), the screen looks like this:

Click on Cancel

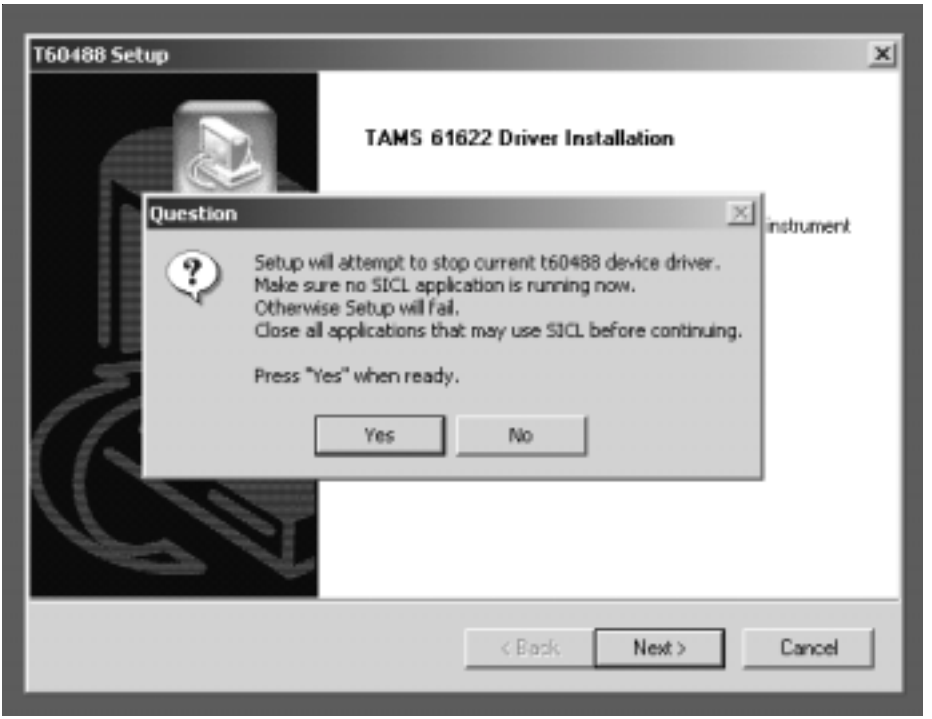
1. Make sure you have privileges enabling you to install device drivers.

2. Insert the CD with the t61622 driver into the CD-ROM drive.

3. Run “setup.exe” from the CD directory “WXP_VERx.xx”.

4. Follow the instructions on the screen.

You may or may not get the following message:



5. Click on Yes and/or Next and continue with the instructions on the screen.

6. Finally, the installation program will ask you to reboot your PC. Please go ahead and do so.

After rebooting you will be prompted with the following screen:

Click on Next

Finally you will get a screen that looks like this:

Click on Finish.

After this your TAMS 61622 GPIO card should be ready to be configured. Please follow the instructions in the next section.

Configuring the Card in Windows NT4.0 / 2000 / XP

1. Make sure that the HP/Agilent SICL software package, TAMS 61622 card(s) and the t61622 driver are installed and the computer rebooted.

2. Configure the interface by executing the IO Config program, which will now be located in the SICL/bin subdirectory. You should also have a shortcut under Start-> Programs-> Agilent IO Libraries

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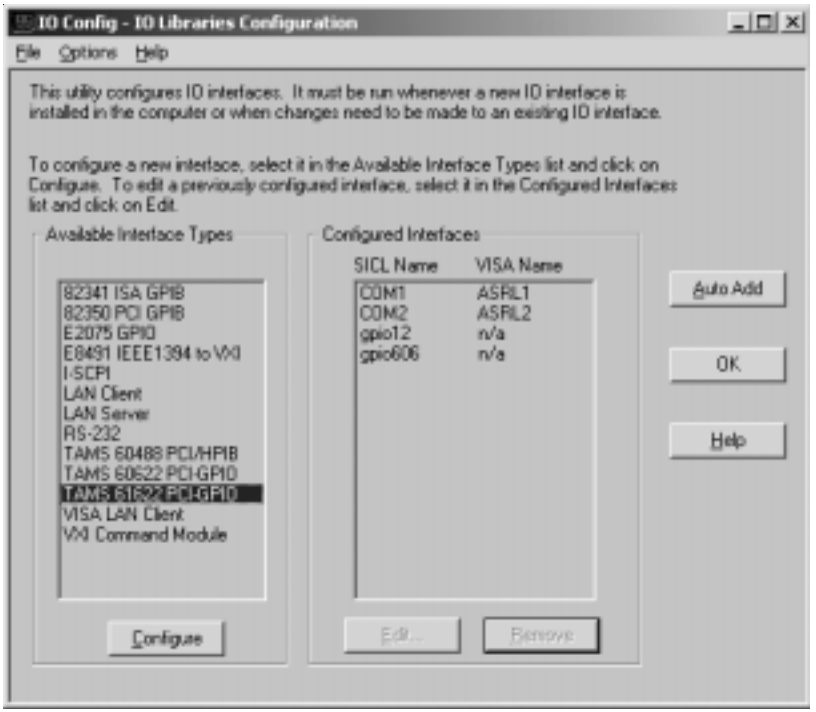
Note: Configuration of TAMS 61622 interface assumes knowledge of SICL configuration procedures specific to the platform. Refer to SICL documentation.

If the Agilent IO Libraries were installed using the default values the SICL\bin subdirectory will be found here:

Window NT: C:\SICLNT\bin or C:\SICL\bin\

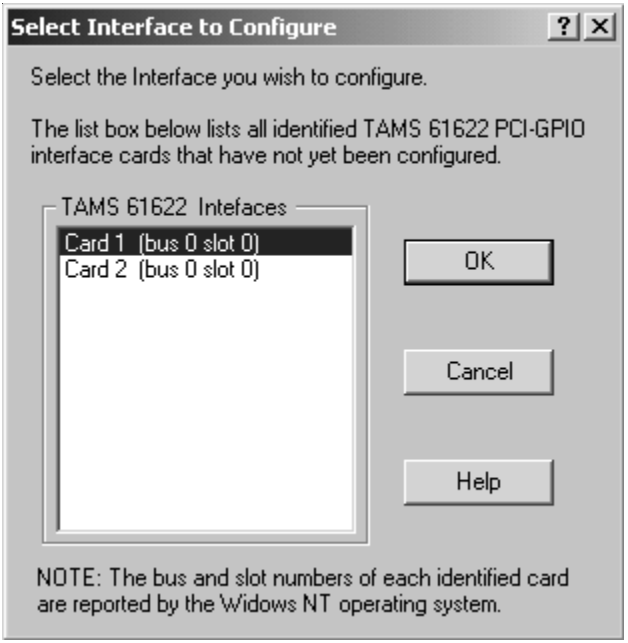
Windows 2000 / XP: C:\Program Files\Agilent\IO Libraries\bin\

Upon execution, the IO Config program will present a window like this:



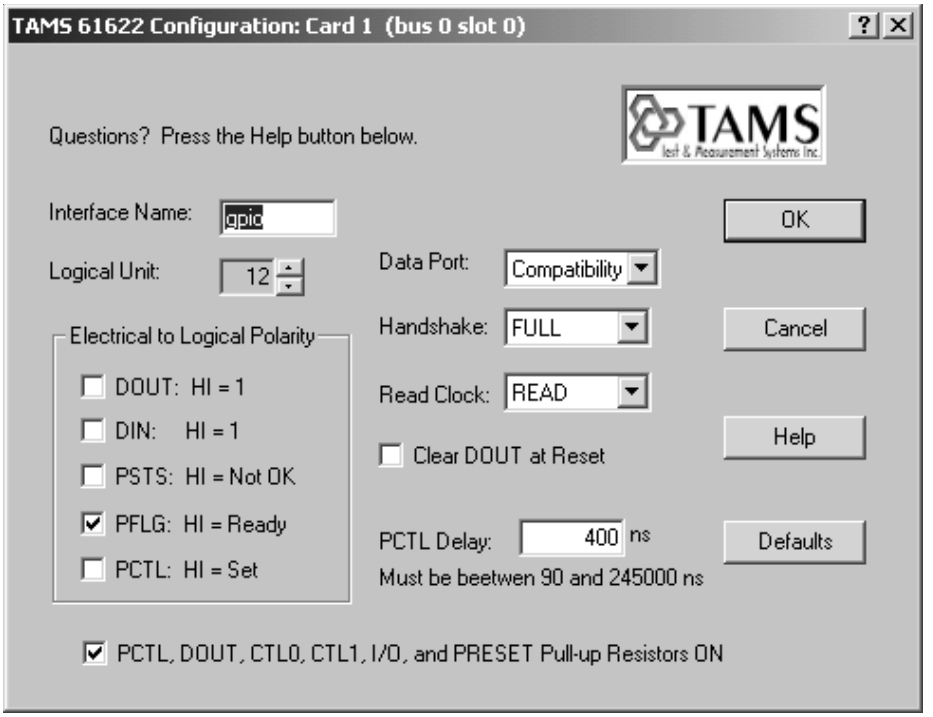
3. In the “Available Interface Types” list box select “TAMS 61622 PCI-GPIO” and click Configure button.

4. If more than one 61622 card is present on the system, select the card to configure. (If more than one card is present the following window will appear. if you have only one card continue to the next step):



5. Select the 61622 card you wish to configure (if you have one card only, you will not need to select any card, the system will do it automatically for you).

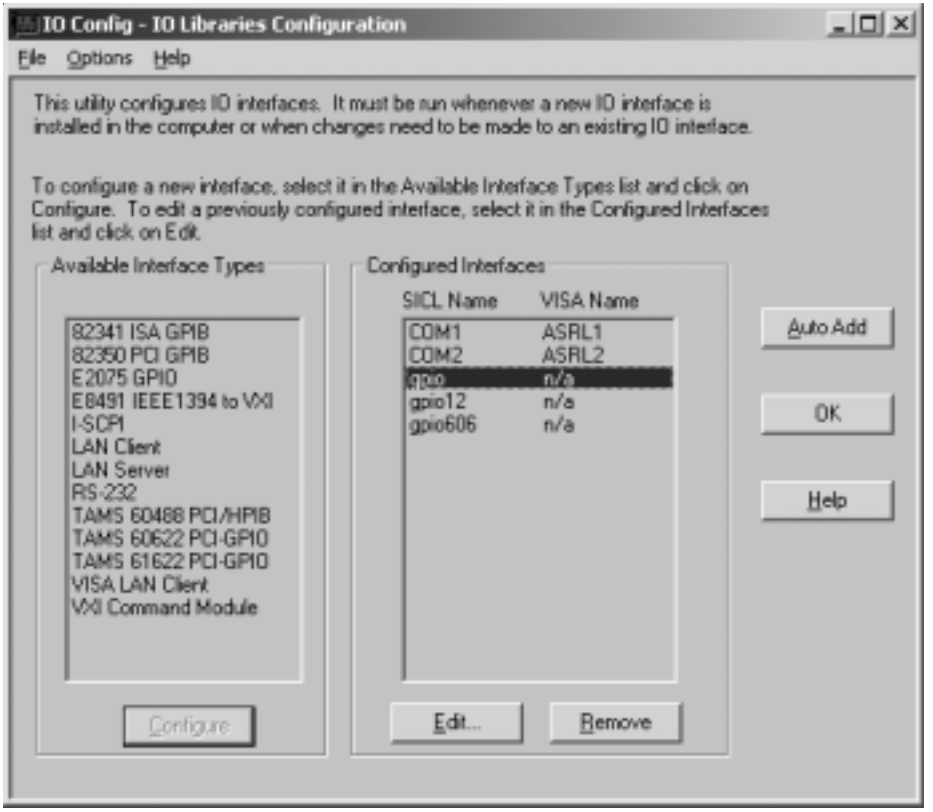
6. Click on OK. Now the following window will appear:



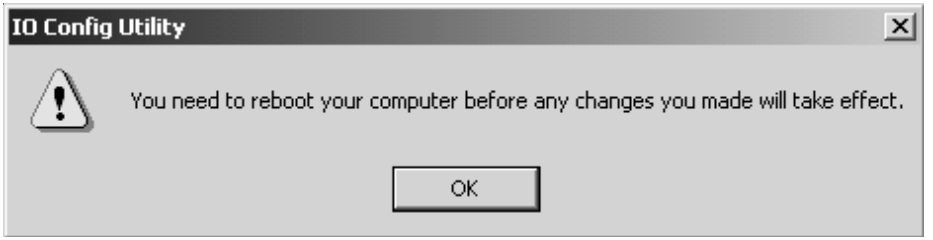
7. Modify or accept default configuration parameters. For context sensitive help click on the Help button or press the F1 key.

8. When you are finished setting the configurable parameter, dismiss the dialog box by clicking the OK button.

9. You will see your interface listed on the screen, such as:



10. Click OK. You will get a window like this:



11. Please click on OK but do not reboot your system as this message is intended for ISA cards not PCI cards.

Configuration Information

This section provides a detailed, functional description of the TAMS 61622 GPIO interface. You will need to understand this information in order to set the appropriate configuration values for the TAMS 61622. This information should also be helpful when you are preparing and installing the GPIO cable.

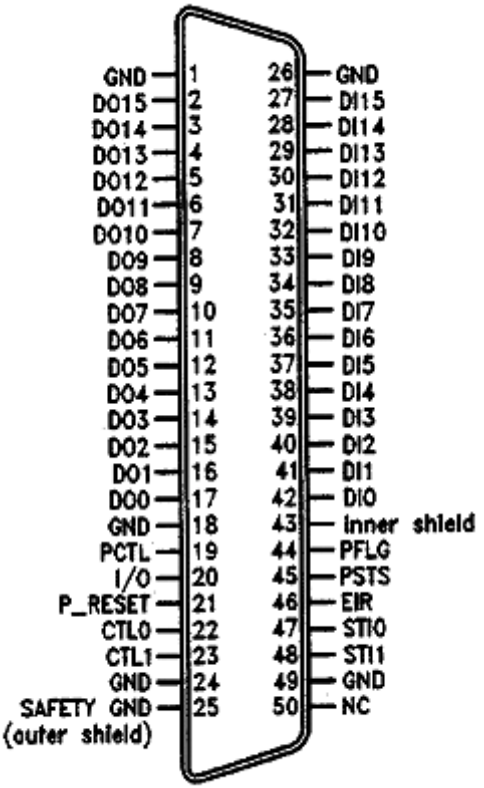
After you have read this section and decided how you want to configure the TAMS 61622, refer to your software documentation to configure your I/O application software for the TAMS 61622. (See the “Related Software Documentation” section of this guide.)

This section contains the following :

- Connector Pinouts
- Data Lines
- Peripheral Information Lines:
  - Peripheral Control and Peripheral Flag Handshake Lines (PCTL and PFLG)
  - Input/Output Direction Control Line (I/O)
  - Peripheral Status Line (PSTS)
  - Peripheral Reset Line (P_RESET)
  - External Interrupt Request Line (EIR)
  - Control Output Lines (CTL0 and CTL1)
  - Status Input Lines (STI0 and STI1)
- Direct Memory Access (DMA)

Connector Pinouts

The following figure shows you the Pinouts on the TAMS 61622 GPIO interface connector.



TAMS 61622 GPIO Connector Pinouts

Label	Line(s)
DI0 through DI15	Data Input
DO0 through DO15	Data Output
PCTL and PFLG	Peripheral Control and Peripheral Flag handshake
I/O	Input/Output direction control
PSTS	Peripheral Status
P_RESET	Peripheral Reset
EIR	External Interrupt Request
CTL0 and CTL1	Control Output
STI0 and STI1	Status Input
PIN 50	+5 Volts DC current limited to 0.75 A

Key Differences between TAMS 61622 & HP 2074/5

TAMS 61622 PCI DMA.

The TAMS 61622 interface has two modes of transfer: DMA and interrupt driven. A program may control transfer mode used by calls to ***ihint()***. See the *HP/ Agilent SICL Reference Manual* for more information.There are six values that could be specified to this call:

I_HINT_USEPOLL

I_HINT_USEINTR

I_HINT_USEDMA

I_HINT_IO

I_HINT_SYSTEM

I_HINT_DONTCARE

If I_HINT_USEPOLL is specified, interrupt mode (I_HINT_USEINTR) is used. This is due to the fact that with advances in hardware and operating systems, there is no situation that using polled mode would have advantage over interrupt mode. Interrupt mode is not noticeably slower than polled and it releases the processor while waiting for interrupts greatly improving system overall performance.

If I_HINT_USEINTR is used, all inbound and outbound transfer will be performed in interrupt mode. Each transfer of a single 8 or 16-bit data item (depending on configured GPIO width) will be initiated, and processor freed to perform other tasks. Once the transfer is complete, the processor will initiate another transfer.

If the transfer is inbound and a termination and/or end character is specified, before initiating another transfer the driver will check if the termination condition occurred.

The `igpioctrl(id, I_GPIO_READ_EOI, <end_char>)` and `itermchr(id, <term_chr>)` calls control end and termination characters.

If I_HINT_USEDMA is specified, DMA will always be used for outbound transfer. For inbound transfer, if no termination nor end character is specified, DMA is used. Otherwise interrupt mode (I_HINT_USEINTR) will be used. This will only happen for the current transfer. No call to ***ihint()*** is required to restore DMA transfer mode. For the next transfer, DMA will be resumed for outbound and if no termination and/or end character is specified, for inbound transfers.

If I_HINT_IO or I_HINT_SYSTEM or I_HINT_DONTCARE is specified, then DMA (I_HINT_USEDMA) with be used. The I_HINT_IO is intended for best transfer performance and I_HINT_SYSTEM for most system performance executing other applications. The fact is that both qualities are delivered best when DMA is used.

However, there is a difference between above three modes and I_HINT_USEDMA. It is possible for PCI bus DMA transfer to fail due to hardware or OS instabilities. If this happens, The three modes described in this paragraph will switch from that moment to interrupt mode (I_HINT_USEINTR) until the computer is rebooted. An explicit ***ihint()*** call with I_HINT_USEDMA will always use DMA; and, if a DMA bus error occurs, the iread or iwrite will return with an error.

However, the PCI bus DMA error is very unlikely to occur.

TAMS 61622 PCTL delay.

The TAMS 61622 is much more flexible than any other available GPIO interface. With the HP 2074/5 interface a user has a choice of one of eight delay time values. The gaps between those values are significant and prevent performance optimization. The TAMS 61622 accepts values directly in nanoseconds. The range extends from 90 nanoseconds to 245000 nanoseconds (245 microseconds) allowing optimal transfer performance according to the length of cable used. In addition, the time specified is applied with accuracy at any mode of transfer, while other available GPIO interfaces add as much as 500 ns when different modes are used. This caused users to configure more PCTL time than actually required in order to compensate for worst possible transfer mode cases.

The TAMS 61622 PCTL delay is configurable by running the iocfg32.exe utility (Windows), or it may be changed at any time from within an application by a call to `igpioctrl(id, I_GPIO_PCTL_DELAY, <val>)` where *<val>* could be one of eight HP 2074/5 compatible values, or directly a value in nanoseconds between 90 and 245000 inclusive.

The eight (0-7) of HP 2074/5 compatible values are interpreted as follows:

0 - 200ns, 1 - 400ns, 2 - 700ns, 3 - 1.2us, 4 - 2us, 5 - 5us, 6 - 10us, 7 - 50us.

Booting after configuring is not required with TAMS 61622.

When TAMS 61622 PCI GPIO card is configured via the SICL configuration it does not require rebooting to take effect. Always choose Cancel or No button when prompted to reboot the machine.

Changes take effect when a session on a newly configured interface is started for the first time within a process.

Care should be taken when a running application uses TAMS 61622 interface while it is configured.

If, for example, a polarity is changed on an interface while an application uses it, it may take effect in the middle of a transfer causing undesired effects. However, no fatal effects like system crash or device hang could be caused.

Note: On Windows, rebooting is required only once after t61622 driver installation.

Appendix A: Wiring

Data Lines

There are 32 data lines on the TAMS 61622: 16 designated as data input, and 16 designated as data output. Color codes are provided for TAMS 622-001 GPIO cable and HP 5061-4209 GPIO cable.

Data Input Lines

The 16 data input lines are labeled DIO through DI15. The following tablelists the connector pin numbers and cable wire color codes for the data input lines.

Data Input Lines

Label	Pin No.	622-001	5061-4209
DI0	42	White on Grey	Black
DI1	41	Brown on Blue	Brown
DI2	40	White on Violet	Red
DI3	39	White on Blue	Orange
DI4	38	White on Green	Yellow
DI5	37	White on Yellow	Green
DI6	36	White on Orange	Blue
DI7	35	White on Pink	Violet
DI8	34	Brown on Green	White/Brown/Red
DI9	33	Brown on Yellow	White/Brown/Orange
DI10	32	Brown on Orange	White/Brown/Yellow
DI11	31	Brown on Pink	White/Brown/Green
DI12	30	Tan on Grey	White/Red/Orange
DI13	29	Tan on Violet	White/Red/Yellow
DI14	28	Tan on Blue	White/Red/Green
DI15	27	Tan on Green	White/Red/Blue

Data Output Lines

The 16 data output lines are labeled DO0 through DO15. The following table lists the connector pin numbers and wire color codes for the data output lines.

Data Output Lines

Label	Pin No.	622-001	5061-4209
DO0	17	Grey on White	White/Black
DO1	16	Blue on Brown	White/Brown
DO2	15	Violet on White	White/Red
DO3	14	Blue on White	White/Orange
DO4	13	Green on White	White/Yellow
DO5	12	Yellow on White	White/Green
DO6	11	Orange on White	White/Blue
DO7	10	Pink on White	White/Violet
DO8	9	Green on Brown	White/Orange/Yellow
DO9	8	Yellow on Brown	White/Orange/Green
DO10	7	Orange on Brown	White/Orange/Blue
DO11	6	Pink on Brown	White/Orange/Violet
DO12	5	Grey on Tan	White/Yellow/Green
DO13	4	Violet on Tan	White/Yellow/Blue
DO14	3	Blue on Tan	White/Yellow/Violet
DO15	2	Green on Tan	White/Yellow/Gray

Peripheral Information Lines

The following table lists the connector pin numbers and wire color codes for the peripheral information lines.

Peripheral Information Lines

Label	Pin No.	622-001	5061-4209
GRD	1	Yellow on Tan	
GRD	18	Violet on Brown	
PCTL	19	Tan on White	White/Grey
I/O	20	Grey on Brown	White/Black/Brown
P_RESET	21	Orange on Pink	White/Black/Red
CTL0	22	Brown on Tan	White/Red/Violet
CTL1	23	Pink on Tan	White/Red/Grey
GRD	24	Brown on White	
Safety GRD	25	Orange on Tan	
GRD	26	Tan on Yellow	
Safety GRD	42	Brown on Violet	
PFLG	44	White on Tan	Grey
PSTS	45	Brown on Grey	White/Black/Grey
EIR	46	Pink on Orange	White/Brown/Grey
STI0	47	Tan on Brown	White/Brown/Blue
STI1	48	Tan on Pink	White/Brown/Violet
GRD	49	White on Brown	
+5 (fused)	50	Tan on Orange	

Appendix B: TAMS 61622 SICL Extensions

All of the TAMS 61622 SICL extension functions are implemented by using the header file t61622sicl.h and the standard SICL functions igpioctrl and igpiostat.

These two functions are described below:

IGPIOCTRL

Supported sessions: . . . . . **interface**
Affected by functions: . . . . . **ilock, itimeout**

C Syntax

```
#include <sicl.h>
#include <t61622sicl.h>

int igpioctrl (id, request, setting);

INST id;
int request;
unsigned long setting;
```

Visual Basic Syntax

```
Function igpioctrl
(ByVal id As Integer, ByVal request As Integer,
ByVal setting As Long)
```

IGPIOSTAT

Supported sessions: . . . . . **interface**

C Syntax

```
#include <sicl.h>
#include <t61622sicl.h>

int igpiostat (id, request, result);

INST id;
```

```
int request;
unsigned long *result;
```

Visual Basic Syntax

```
Function igpiostat
(ByVal id As Integer, ByVal request As Integer,
ByVal result As Long)
```

The following are all the TAMS 61622 SICL extensions and some examples of how to use them.

TAMS 61622 PCTL delay

The TAMS 61622 PCTL delay function provides a **extended PCTL delay control** that was not available before. Besides the standard 0-7 values for delay used with HP cards, the delay of the TAMS 61622 may be set directly in nanoseconds.

Examples:

Setting the PCTL delay to 560ns

igpioctrl(id, I_GPIO_T61622_DLY_TM, 560)

Reading the PCTL delay in nanoseconds

igpiostat(id, I_GPIO_T61622_DLY_TM, &dtm)

Important time defines for the PCTL delay (in nanoseconds)

T61622_DLY_MIN	90	Minimum for a PCTL delay
T61622_DLY_STP	60	Hardware effective step
T61622_DLY_DFT	400	Value loaded on boot
T61622_DLY_MAX	245700	Maximum for a PCTL delay

TAMS 61622 Filtering

This feature allows filtering of DIN[0..15], STI0, STI1 and EIR lines for glitch rejection.

There are two different request for this function.

I_GPIO_T61622_FLT_EN controls what groups are going to be enabled for filtering. The groups are DIN[0..15], STI[0..1] and EIR.

I_GPIO_T61622_FLT_TM sets the time in nanoseconds for the group or groups that are enabled. The time set is common for all the lines within those groups. No individual lines can be controlled. The defines T61622_DIN,

T61622_STI, and T61622_EIR control DIN[0..15], STI[1..0] and EIR groups respectively.

Examples:

Using **I_GPIO_T61622_FLT_EN**

Enable DIN group for filtering

igpioctrl(id, I_GPIO_T61622_FLT_EN, T61622_DIN);

Read groups are enabled

igpiostat(id, I_GPIO_T61622_FLT_EN, &fen);

Using **I_GPIO_T61622_FLT_TM**

Set filtering to 1 us (microsecond)

igpioctrl(id, I_GPIO_T61622_FLT_TM, 1000)

Read the time set for filtering in nanoseconds

igpiostat(id, I_GPIO_T61622_FLT_TM, &ftm)

Important time defines for line filtering (in nanoseconds)

T61622_FLT_MIN	30	Minimum filtering time
T61622_FLT_STP	60	Hardware effective step
T61622_FLT_DFT	150	Value loaded on boot
T61622_FLT_MAX	15300	Maximum filtering time

TAMS 61622 Polarity

This function allows the setting of **detailed polarity for DIN, STI0, STI1, and EIR.** The polarity of nineteen lines (DIN[0..15], STI[0..1] and EIR) can be controlled independently. It enables interrupt control of either rising or falling edge of a line level transition.

For DIN lines interpretation and implementation of the polarity is identical to the standard GPIO DIN polarity as described in the SICL manuals.

For the STI and EIR lines, standard GPIO does not provide polarity configuration. This is a TAMS 61622 extension to the GPIO.

To maintain maximum compatibility with the standard GPIO, the following rules apply:

- For STI and EIR lines, if polarity is set to 0, their behavior is fully compatible with standard GPIO. If set to 1, polarity is reversed for these lines.
- For DIN lines, 61622 extensions allow to set polarity for each line independently. Setting the DIN polarity with standard GPIO SICL igpioctrl (**`id, I_GPIO_POLARITY, setting`**) is still supported and will cause setting or clearing of all the DIN polarity lines with a single call. This is

because the standard allows only for all the DIN polarity to be set at a time. This guarantees backwards compatibility.

Examples:

Setting polarity for only DIN6 and EIR lines

igpioctrl(id, I_GPIO_T61622_POL, T61622_DIN06 | T61622_EIR)

Reading back the polarity setting

igpiostat(id, I_GPIO_T61622_POL, &pol);

TAMS 61622 Latching

This function allows latching the levels of the lines enabled, in the three different groups **DIN[0..15], STI0, STI1, and EIR lines**, in two different fashions depending on what polarity is set for each line in each group (please refer to point 3: TAMS 61622 Polarity).

- polarity set to 0, the latch will occur on a LO to HI (logically) transition.
- polarity set to 1, the latch will occur on a HI to LO (logically) transition.
- This function has three different requests:
- **I_GPIO_T61622_LAT_EN** controls which group of lines are enabled for latching, DIN[0..15], STI0, STI1 and/or EIR.
- **I_GPIO_T61622_LAT_RD** lets you read the latched lines.
- **I_GPIO_T61622_LAT_CL** clears the latched lines.

Examples:

Enable T61622_DIN06 and T61622_EIR

igpioctrl (id, I_GPIO_T61622_LAT_EN, T61622_DIN06 | T61622_EIR)

Read who is enabled for latching

igpiostat(id, I_GPIO_T61622_LAT_EN, &len)

Read latched lines

igpiostat(id, I_GPIO_T61622_LAT_RD, &lat)

Clear latched lines

igpioctrl(id, I_GPIO_T61622_LAT_CL, lat)

TAMS 61622 line interrupt

This function controls which lines can cause an interrupt**. Interrupts on level transitions on DIN[0..15], STI[0..1] and EIR lines** can be controlled individually. The interrupt occurs on LO to HI (logically) transition on a GPIO

line assuming polarity set to 0, or HI to LO transition if polarity is set to 1 (please refer to point 3: TAMS 61622 Polarity).

If this function is combined with the TAMS 61622 latching function, then the interrupt will fire only once. If this is the case, the latched lines need to be cleared before other interrupts could happen from those lines.

If one or more interrupts occur, the interrupt handler is called with the “reason” parameter equal to I_INTR_GPIO_T61622 and the “sec” parameter is the mask of the lines that interrupted.

The mask is always a subset of the following:

T61622_DIN | T61622_STI | T61622_EIR | T61622_RDY

Examples:

Enabling DIN4 line to interrupt

igpioctrl(id, I_GPIO_T61622_INT_EN, T61622_INT_DIN04)

Checking what lines can interrupt

igpiostat(id, I_GPIO_T61622_INT_EN, &int)

TAMS 61622 Pull-up

I_GPIO_T61622_PUL controls if DOUT[0..15], CTL[0..1], PCTL, I/O, and PRESET lines are pulled up with 4.7k resistors to +5V. There is no control for individual lines. All lines are controlled at the same time.

Examples:

Turn all pull-ups ON

igpioctrl(id, I_GPIO_T61622_PUL, 1)

Check if pull-ups are on

igpiostat(id, I_GPIO_T61622_PUL, &pull)

Turn pull-ups OFF

igpioctrl(id, I_GPIO_T61622_PUL, 0)

TAMS 61622 Board ID

The 61622 is equipped with a rotary switch. This switch is set by the user. The purpose is identification of each GPIO board on a system with multiple GPIO cards. This feature is especially useful if multiple boards are residing on a PCI bridge since some PCI bridges do not provide a reliable way for PCI slot identification.

This switch has no effect on the GPIO functionality itself.

The user would set the switch position to a unique value for each card on the system and then can read its value by using the request **I_GPIO_T61622_CID** to check which physical card has an opened session.

Examples:

Get the switch value

igpiostat(id, I_GPIO_T61622_CID, &swID)

TAMS 61622 Handshake

TAMS t61622 internal handshaking loop makes easier to test/debug GPIO applications without having anything connected to the TAMS 61622 GPIO card.

This test mode only has an effect on handshaking transfers. If the mode is on, the PCTL/PFLG get in a loop mode and as a consequence no external device is needed for the handshaking because it is being generated internally by the TAMS 61622 card.

The user can turn the mode on or off by using the request **I_GPIO_TEST_ONLY.** If an unsupported value is passed it is ignored. The actual polarity of PCTL and PFLG lines does not affect the internal handshaking loop mode.

Examples:

Enable loop test mode

igpioctrl(id, I_GPIO_TEST_ONLY, T61622_HSHK_LOOP)

Get test settings

igpiostat(id, I_GPIO_TEST_ONLY, &test)

Disable loop test mode

igpioctrl(id, I_GPIO_TEST_ONLY, 0)

Important time defines for loop test mode

T61622_HSHK_LOOP	0x00000001	loop PFLG and PCTL
T61622_DLY_NONE	0x00000002	loop with no delay
T61622_HSHK_NONE	0x00000004	loop with no handshaking

TAMS 61622 DOUT read

The **I_GPIO_T61622_DOUT** reads the value of DOUT lines. The value read is not affected by the DOUT polarity.

Example:

Get the DOUT value

igpiostat(id, I_GPIO_T61622_DOUT, &dout)

TAMS 61622 Macros

The following is a table with all of the defines passed to the TAMS 61622 SICL extension functions that you can use. Individual bits could be passed to select specific line(s).

TAMS 61622 SICL extension function defines

T61622_DIN	0x0000FFFF	DIN[0..15] 16 bits
T61622_DIN_L	0x000000FF	DIN[0..7] 8 bits
T61622_DIN_U	0x0000FF00	DIN[8..15] 8 bits
T61622_STI	0x00030000	STI[0..1] 2 bits
T61622_EIR	0x00040000	EIR 1 bit
T61622_RDY	0x00080000	RDY 1 bit
T61622_MORE	0x00100000	used inside driver only
T61622_ALL	0x000FFFFF	all of above 20 bits

Individual bits for DIN and STI

T61622_DIN00	0x00000001
T61622_DIN01	0x00000002
T61622_DIN02	0x00000004
T61622_DIN03	0x00000008
T61622_DIN04	0x00000010
T61622_DIN05	0x00000020
T61622_DIN06	0x00000040
T61622_DIN07	0x00000080
T61622_DIN08	0x00000100
T61622_DIN09	0x00000200
T61622_DIN10	0x00000400
T61622_DIN11	0x00000800
T61622_DIN12	0x00001000
T61622_DIN13	0x00002000
T61622_DIN14	0x00004000
T61622_DIN15	0x00008000
T61622_STI0	0x00010000
T61622_STI1	0x00020000

Warranty Information

ONE YEAR LIMITED WARRANTY

Test & Measurement Systems, Inc. warrants to the purchaser that the Interface card will be free of all defects in material and/or workmanship for one year from the date of shipment to the customer.

In the event of malfunction or failure attributable directly to faulty material and/or workmanship, TAMS will at it's option, repair or replace the defective product or components, to whatever extent it shall deem necessary to restore the product or component, to proper operating condition. TAMS may at its option repair or replace, a defective unit with a new or refurbished unit.

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